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Delay optimization of linear depth boolean circuits with prescribed input arrival times

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Abstract

We consider boolean circuits C over the basis $\Omega = \{\vee, \wedge\}$ with inputs $x_1, x_2, \ldots, x_n$ for which arrival times $t_1, t_2, \ldots, t_n \in \mathbb{N}_0$ are given. For $1 \leqslant i \leqslant n$ we define the delay of x_i in C as the sum of t_i and the number of gates on a longest directed path in C starting at x_i. The delay of C is defined as the maximum delay of an input.

Given a function of the form

$$f(x_1, x_2, \ldots, x_n) = g_{n-1}(g_{n-2}(\ldots g_3(g_2(g_1(x_1, x_2), x_3), x_4) \ldots, x_{n-1}), x_n)$$

where $g_j \in \Omega$ for $1 \leqslant j \leqslant n-1$ and arrival times for $x_1, x_2, \ldots, x_n$, we describe a cubic-time algorithm that determines a circuit for f over Ω that is of linear size and whose delay is at most 1.44 times the optimum delay plus some small constant.

Keywords: Circuit; Straight-line program; Depth; Delay; Computer arithmetic; VLSI design

1. Motivation

The motivation for the present work is a problem in VLSI design. At one of the final stages in the design process of a chip, the tool that performs the so-called static timing analysis [2–4] detects paths of 'negative slack'. These are paths on which the propagation

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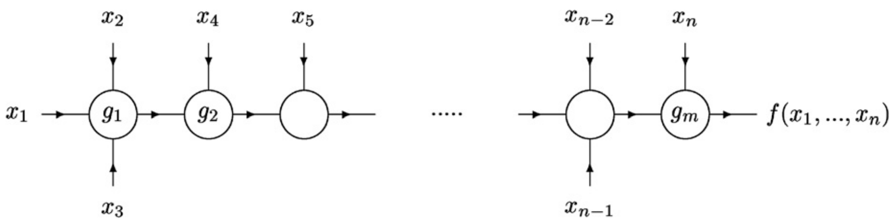

Fig. 1.

of the signal is too slow to guarantee the correct functioning of the chip. The analysis tool reports these paths, which usually consist of a sequence of gates $g_1, g_2, \dots, g_m$ that perform some elementary logical operation on their inputs (see Fig. 1).

The output of the final gate g_m is a boolean function $f(x_1, \dots, x_n)$ of the inputs. If we are given an arrival time, say $\mathrm{t}(x_i)$, for each input x_i and a delay, say $\mathrm{d}(g_j)$, for each gate g_j, then static timing analysis will determine the arrival time of the output of gate g_m, i.e., the time at which the evaluation of f terminates, as the maximum, over all paths from an input x_i to the output of g_m, of the sum of $\mathrm{t}(x_i)$ and all gate delays along the path. If for example for the path in Fig. 1, $m = 3$, g_1 is a 3-and, g_2 is a 2-or and g_3 is a 2-nand (for undefined terminology we refer to [9] or [12]), then $f(x_1, x_2, x_3, x_4, x_5) = \neg(((x_1 \wedge x_2 \wedge x_3) \vee x_4) \wedge x_5)$ and the evaluation of f terminates at

$$\max\bigl\{\mathrm{t}(x_1) + \mathrm{d}(g_1) + \mathrm{d}(g_2) + \mathrm{d}(g_3), \mathrm{t}(x_2) + \mathrm{d}(g_1) + \mathrm{d}(g_2) + \mathrm{d}(g_3),$$
$$\mathrm{t}(x_3) + \mathrm{d}(g_1) + \mathrm{d}(g_2) + \mathrm{d}(g_3), \mathrm{t}(x_4) + \mathrm{d}(g_2) + \mathrm{d}(g_3), \mathrm{t}(x_5) + \mathrm{d}(g_3)\bigr\}.$$

In order to guarantee that the chip works correctly, we have to find a faster representation of f. This leads us to the algorithmical problem which we state more precisely in the next section.

2. Problem

We consider boolean circuits [9,12] over the basis $\Omega = \{\vee, \wedge\}$ whose elements have fan-in 2 for functions $f : \{0, 1\}^n \to \{0, 1\}$ of the form

$$f(x_1, x_2, \dots, x_n) = g_{n-1}(g_{n-2}(\dots g_3(g_2(g_1(x_1, x_2), x_3), x_4) \dots, x_{n-1}), x_n) \tag{1}$$

where $g_j \in \Omega$ for $1 \leqslant j \leqslant n - 1$. Clearly, (1) immediately leads to a similar circuit as in Fig. 1.

If we are given a non-negative integer arrival time $t_i \in \mathbb{N}_0 = \{0, 1, 2, \dots\}$ for input x_i for $1 \leqslant i \leqslant n$, then we define the *delay* $\mathrm{delay}(x_i)$ of x_i in some circuit C as the sum of t_i and the number of gates on a longest directed path in C starting at x_i. The *delay* $\mathrm{delay}(C)$ of C is defined as the maximum delay of an input in C. Given a function f and arrival times as above, we denote the minimum delay of a circuit for f by $\mathrm{delay}(f)$. For some first and fundamental results on this notion of delay we refer the reader to [8].

There is a simple lower bound on the achievable delay extending a classical observation of Winograd [13].

Lemma 1. *If* $f:\{0,1\}^n \to \{0,1\}$ *is computable over* Ω *and dependent on each of its inputs* $x_1, x_2, \dots, x_n$*, which have arrival times* $t_1, t_2, \dots, t_n \in \mathbb{N}_0$*, then*

$$\mathrm{delay}(f) \geqslant \left\lceil \log_2\left(\sum_{i=1}^{n} 2^{t_i}\right)\right\rceil. \tag{2}$$

Proof. The existence of a circuit C for f over Ω with delay T implies the existence of a rooted binary tree with n leaves of depths at most $(T-t_1), (T-t_2), \dots, (T-t_n) \in \mathbb{N}_0$. By Kraft's inequality, such a tree exists if and only if $\sum_{i=1}^{n} 2^{-(T-t_i)} \leqslant 1$ or, equivalently, $T \geqslant \log_2(\sum_{i=1}^{n} 2^{t_i})$, and the proof is complete. □

Note that if $f(x_1, x_2, \dots, x_n) = \bigvee_{i=1}^{n} x_i$ or $f(x_1, x_2, \dots, x_n) = \bigwedge_{i=1}^{n} x_i$, then a tree as considered in the above proof immediately leads to a circuit for f of minimum delay and can obviously be constructed in polynomial time (see [8]).

Our main result is a cubic-time dynamic programming algorithm that produces a circuit for functions f as in (1) whose delay is at most about 1.44 times the value of the lower bound (2). We describe this algorithm first for the function $f_0:\{0,1\}^{2n} \to \{0,1\}$ with

$$f_0(x_1, y_1, x_2, y_2, \dots, x_n, y_n) = ((\dots(((x_1 \wedge y_1) \vee x_2) \wedge y_2) \vee \dots) \vee x_n) \wedge y_n. \tag{3}$$

The function f_0 is known in computer arithmetic [10,11]. It can be used to perform the carry-bit calculation for the addition of two n-bit binary numbers (for details see [9]). As part of their circuits for addition Brent [1] and Khrapchenko [5] both described circuits for f_0 of depth $\log_2(n) + \mathrm{O}(\sqrt{\log(n)})$ (cf. also [6]). Nevertheless, their original constructions and analysis hardly generalize to the case of arrival times and would certainly not lead to polynomial time algorithms.

The existence of relevant signal arrival time differences has been acknowledged in some recent engineering publications [7,14] that propose constructions for binary adders taking these differences into account. The greedy approaches used by Liu et al. [7] and Yeh and Jen [14] lead to adders for two n-bit binary numbers that are of size $\mathrm{O}(n^2)$ but for which no delay bound has been proved. Our algorithm allows the construction of an adder for two n-bit binary numbers which is also of quadratic size but provably has at most about 1.44 times the minimum delay. In [8] we describe circuits for the prefix problem taking arrival times into account which immediately leads to adders for two n-bit binary numbers which are of size $\mathrm{O}(n \log(\log(n)))$ and have at most about twice the minimum delay.

In Section 3 we first describe the algorithm for functions as in (3). In Section 4, we analyse the delay of the circuits constructed in Section 3. In Section 5, we describe the algorithm for functions as in (1) and state the main result. Finally, in Section 6 we make some concluding remarks.

3. Algorithm for f_0 as in (3)

For $1 \leqslant l \leqslant n-1$ the function f_0 satisfies the following identity.

$$f_0(x_1, y_1, x_2, y_2, \dots, x_n, y_n)$$

$$
\begin{aligned}
&= ((\ldots(((x_1 \wedge y_1) \vee x_2) \wedge y_2) \vee \ldots) \vee x_n) \wedge y_n \\
&= ((\ldots((((x_1 \wedge y_1 \wedge y_2) \vee (x_2 \wedge y_2)) \vee x_3) \wedge y_3)\ldots) \vee x_n) \wedge y_n \\
&= \ldots \\
&= \bigvee_{i=1}^{n}\left(x_i \wedge \bigwedge_{j=i}^{n} y_j\right) \\
&= \left(\left(\bigvee_{i=1}^{l}\left(x_i \wedge \bigwedge_{j=i}^{l} y_j\right)\right) \wedge \left(\bigwedge_{j=l+1}^{n} y_j\right)\right) \vee \left(\bigvee_{i=l+1}^{n}\left(x_i \wedge \bigwedge_{j=i}^{n} y_j\right)\right) \\
&= \left(f_0(x_1, y_1, \ldots, x_l, y_l) \wedge \left(\bigwedge_{j=l+1}^{n} y_j\right)\right) \vee f_0(x_{l+1}, y_{l+1}, \ldots, x_n, y_n). \qquad (4)
\end{aligned}
$$

Note that we commit a small *abus de langage* using 'f_0' to denote formally different functions. We now describe the algorithm for f_0.

Algorithm 1.
Input: Integers $n \in \mathbb{N} = \{1, 2, \ldots\}$ and $t_1, s_1, t_2, s_2, \ldots, t_n, s_n \in \mathbb{N}_0$.
Output: A circuit $C_0(t_1, s_1, t_2, s_2, \ldots, t_n, s_n)$ over Ω with inputs $x_1, y_1, \ldots, x_n, y_n$ that has the two outputs $f_0(x_1, y_1, x_2, y_2, \ldots, x_n, y_n)$ and $\bigwedge_{j=1}^{n} y_j$.

In what follows, we use t_i as the arrival time for x_i and s_i as the arrival time for y_i for $1 \leqslant i \leqslant n$. Furthermore, we denote the subcircuit of $C_0(t_1, \ldots, s_n)$ that computes $f_0(x_1, \ldots, y_n)$ by $C_{0,f_0}(t_1, \ldots, s_n)$ and the subcircuit of $C_0(t_1, \ldots, s_n)$ that computes $\bigwedge_{j=1}^{n} y_j$ by $C_{0,\wedge}(t_1, \ldots, s_n)$.

Step 1 If $n = 1$, then let the circuit $C_0(t_1, s_1)$ be as in Fig. 2.

Step 2 If $n \geqslant 2$, recursively construct $C_0(t_1, \ldots, s_n)$ using $C_0(t_1, \ldots, s_l)$ and $C_0(t_{l+1}, \ldots, s_n)$ for some $1 \leqslant l \leqslant n-1$ such that

$$\max\bigl\{\mathrm{delay}\bigl(C_{0,f_0}(t_1, \ldots, s_l)\bigr) + 1, \mathrm{delay}\bigl(C_{0,f_0}(t_{l+1}, \ldots, s_n)\bigr)\bigr\}$$

is minimized.

The output of $C_{0,f_0}(t_1, \ldots, s_n)$ is calculated exactly as in (4) with one $\wedge$-gate and one $\vee$-gate using the output of $C_{0,f_0}(t_1, \ldots, s_l)$, the output of $C_{0,f_0}(t_{l+1}, \ldots, s_n)$ and the output of $C_{0,\wedge}(t_{l+1}, \ldots, s_n)$.

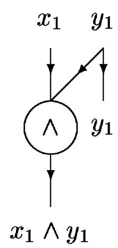

Fig. 2.

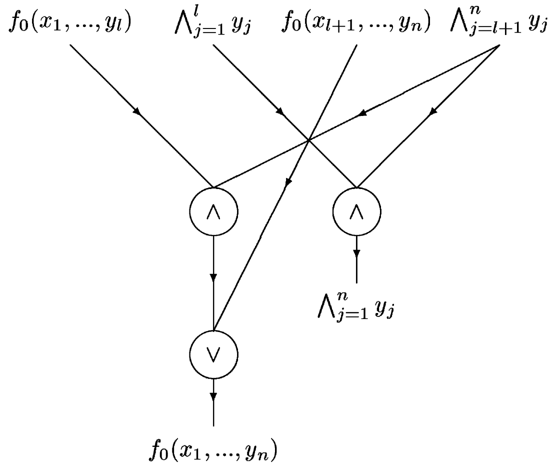

Fig. 3. $C(x_1, \ldots, y_n)$.

Furthermore, the output of $C_{0,\wedge}(t_1, \ldots, s_n)$ is calculated with one $\wedge$-gate using the output of $C_{0,\wedge}(t_1, \ldots, s_l)$ and the output of $C_{0,\wedge}(t_{l+1}, \ldots, s_n)$. See Fig. 3 for an illustration.

We collect some observations in the following lemma.

Lemma 2.

(i) *Algorithm* 1 *works correctly.*
(ii) *The number of* $\vee$*- or* $\wedge$*-gates in* $C_0(t_1, \ldots, s_n)$ *is* $4n - 3$.
(iii) *In* $C_0(t_1, \ldots, s_n)$ *all inputs have fan-out at most* 3 *and all* $\wedge$*- or* $\vee$*-gates have fan-out at most two.*
(iv) $\text{delay}(C_{0,f_0}(t_1, s_1)) = \max\{t_1, s_1\} + 1$.
(v) $\text{delay}(C_{0,\wedge}(t_1, \ldots, s_n)) \leqslant \text{delay}(C_{0,f_0}(t_1, \ldots, s_n)) - 1$.
(vi) $\text{delay}(C_{0,f_0}(t_1, \ldots, s_n))$ *equals*

$$\min_{1 \leqslant l \leqslant n-1} \max\bigl\{\text{delay}\bigl(C_{0,f_0}(t_1, \ldots, s_l)\bigr) + 2, \text{delay}\bigl(C_{0,f_0}(t_{l+1}, \ldots, s_n)\bigr) + 1\bigr\}.$$

(vii) *Algorithm* 1 *can be implemented to run in cubic time.*

Proof. (i) follows from (4). (ii), (iii) and (iv) are obvious. (v) follows easily by induction and immediately implies (vi). (vii) is valid, since Algorithm 1 only needs to calculate the delays of the $\binom{n}{2}$ circuits $C_{0,f_0}(t_i, s_i, \ldots, t_j, s_j)$ for $1 \leqslant i < j \leqslant n$ using the recursion given by (iv) and (vi). This can clearly be done in cubic time. □

In order to analyse the quality of the construction we study the recursion in Lemma 2(iv) and (vi) in the next section.

4. Growth

For $n \geqslant 2$ and non-negative integers a, b, a_1, $b_1, \dots, a_n$, $b_n \in \mathbb{N}_0$ let $\mathcal{D}_0$ be defined recursively by

$$\mathcal{D}_0(a,b) = \max\{a,b\} + 1,$$
$$\mathcal{D}_0(a_1,b_1,\dots,a_n,b_n) = \min_{1 \leqslant l \leqslant n-1} \max\bigl\{\mathcal{D}_0(a_1,b_1,\dots,a_l,b_l) + 2, \\ \mathcal{D}_0(a_{l+1},b_{l+1},\dots,a_n,b_n) + 1\bigr\}. \tag{5}$$

Clearly, this corresponds to the recursion in Lemma 2. If we define $\mathcal{D}_1$ similarly by

$$\mathcal{D}_1(a) = a,$$
$$\mathcal{D}_1(a_1,\dots,a_n) = \min_{1 \leqslant l \leqslant n-1} \max\bigl\{\mathcal{D}_1(a_1,\dots,a_l) + 2, \mathcal{D}_1(a_{l+1},\dots,a_n) + 1\bigr\}, \tag{6}$$

then the following properties are immediate. In order to simplify our notation we write (A,B) to denote the vector $(a_1,a_2,\dots,a_{n_A},b_1,b_2,\dots,b_{n_B})$ where $A = (a_1,a_2,\dots,a_{n_A})$ and $B = (b_1,b_2,\dots,b_{n_B})$.

Lemma 3. *Let $a, a_1, a_2, \dots, a_n, a'_1, a'_2, \dots, a'_n, b_1, b_2, \dots, b_n \in \mathbb{N}_0$ be such that $a_i \leqslant a'_i$ for $1 \leqslant i \leqslant n$. Let $A \in \mathbb{N}_0^{n_A}$ and $B \in \mathbb{N}_0^{n_B}$ with $n_A + n_B \geqslant 1$. Then*

(i) $\mathcal{D}_0(a_1,b_1,\dots,a_n,b_n) = \mathcal{D}_1(\max\{a_1,b_1\}+1, \max\{a_2,b_2\}+1, \dots, \max\{a_n,b_n\}+1)$,
(ii) $\mathcal{D}_1(a_1+a, a_2+a, \dots, a_n+a) = \mathcal{D}_1(a_1,a_2,\dots,a_n) + a$,
(iii) $\mathcal{D}_1(a_1,a_2,\dots,a_n) \leqslant \mathcal{D}_1(a'_1,a'_2,\dots,a'_n)$, *and*
(iv) $\mathcal{D}_1(A,B) \leqslant \mathcal{D}_1(A,a,B)$.

Before we proceed to the analysis, we give a combinatorial interpretation for $\mathcal{D}_1$. Let n non-negative integers $a_1,a_2,\dots,a_n \in \mathbb{N}_0$ be given. We consider rooted binary trees with root r in which every left branch is labelled with length 2, every right branch is labelled with length 1 and the leaves are labelled in left-to-right order with $u_1,u_2,\dots,u_n$.

If D denotes the maximum over all $1 \leqslant i \leqslant n$ of the sum of a_i and the total length of the path from u_i to r, then $\mathcal{D}_1(a_1,a_2,\dots,a_n)$ equals the minimum value of D over all such binary trees. See Fig. 4 for some examples of optimal trees where all edges of length 2 are pointing left.

Let F_k denote the kth Fibonacci number, i.e., $F_0 = 0$, $F_1 = 1$ and $F_n = F_{n-1} + F_{n-2}$ for $n \geqslant 2$. For $k \in \mathbb{N}$ let $Z(k)$ denote the vector of k zeros.

Lemma 4. *Let $k \in \mathbb{N}_0$ and $l, n, m \in \mathbb{N}$. Let $A \in \mathbb{N}_0^n$ and $B \in \mathbb{N}_0^m$.*

(i) $\max\{i \in \mathbb{N} \mid \mathcal{D}_1(Z(i)) \leqslant k\} = F_{k+1}$.
(ii) $\mathcal{D}_1(A,l) \leqslant \mathcal{D}_1(A, Z(F_{l+1}))$.
(iii) $\mathcal{D}_1(l,B) \leqslant \mathcal{D}_1(Z(F_{l+2}), B)$.
(iv) $\mathcal{D}_1(A,l,B) \leqslant \mathcal{D}_1(A, Z(F_{l+3}-1), B)$.

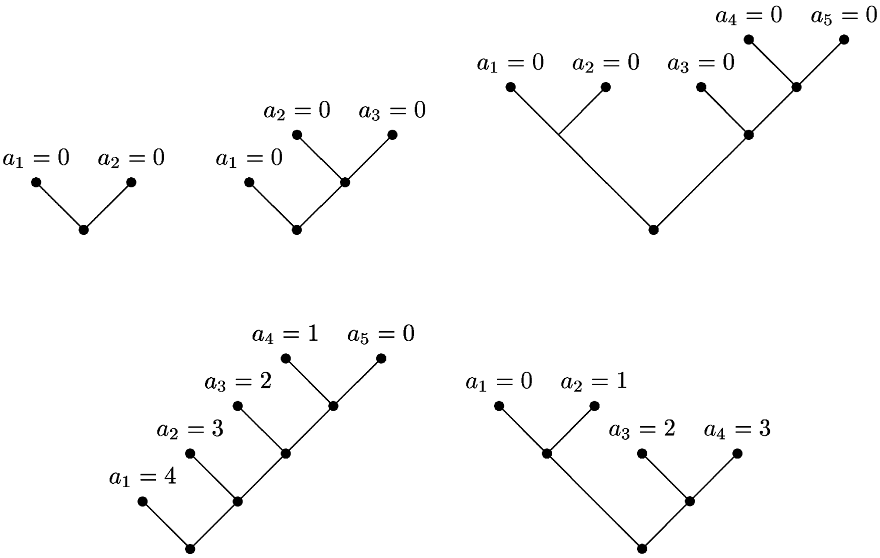

Fig. 4.

Proof. (i) Let $\max(k) = \max\{i \in \mathbb{N} \mid \mathcal{D}_1(Z(i)) \leqslant k\}$. It is easy to verify that $\max(0) = 1$ and $\max(1) = 1$.

By (6), for $l \geqslant 2$ we have $\mathcal{D}_1(Z(l)) = \max\{\mathcal{D}_1(Z(l_1)) + 2, \mathcal{D}_1(Z(l_2)) + 1\}$ for some $l_1, l_2 \in \mathbb{N}$ with $l_1 + l_2 = l$. This immediately implies the recursion $\max(k) = \max(k-2) + \max(k-1)$ for $k \geqslant 2$ and thus we obtain $\max(k) = F_{k+1}$, which completes the proof of (i).

(ii) For contradiction, we assume that (A, l) is a counterexample of minimum length $n+1$.

First, we assume that $\mathcal{D}_1(A, Z(F_{l+1})) = \max\{\mathcal{D}_1(A_1) + 2, \mathcal{D}_1(A_2, Z(F_{l+1})) + 1\}$ for some non-trivial A_1 and some A_2 with $(A_1, A_2) = A$.

If either A_2 is non-trivial or $l \geqslant 2$, then (6) and (i) or the choice of (A, l) imply the contradiction

$$\begin{aligned}\mathcal{D}_1(A, l) &\leqslant \max\bigl\{\mathcal{D}_1(A_1) + 2, \mathcal{D}_1(A_2, l) + 1\bigr\} \\ &\leqslant \max\bigl\{\mathcal{D}_1(A_1) + 2, \mathcal{D}_1\bigl(A_2, Z(F_{l+1})\bigr) + 1\bigr\} \\ &= \mathcal{D}_1\bigl(A, Z(F_{l+1})\bigr).\end{aligned}$$

If A_2 is trivial ($A_1 = A$) and $l = 1$, then $\mathcal{D}_1(A_2, l) + 1 = \mathcal{D}_1(1) + 1 = 2 \leqslant \mathcal{D}_1(A_1) + 2$ and we obtain a similar contradiction.

Therefore, there is some $1 \leqslant r \leqslant F_{l+1} - 1$ such that

$$\mathcal{D}_1\bigl(A, Z(F_{l+1})\bigr) = \max\bigl\{\mathcal{D}_1\bigl(A, Z(F_{l+1} - r)\bigr) + 2, \mathcal{D}_1\bigl(Z(r)\bigr) + 1\bigr\}. \tag{7}$$

By (6), we have $\mathcal{D}_1(A, l) \leqslant \max\{\mathcal{D}_1(A) + 2, l + 1\}$.

If $\mathcal{D}_1(A) + 2 \geqslant l + 1$, then (7) implies the contradiction

$$\mathcal{D}_1(A, l) \leqslant \mathcal{D}_1(A) + 2 \leqslant \mathcal{D}_1\bigl(A, Z(F_{l+1} - r)\bigr) + 2 \leqslant \mathcal{D}_1\bigl(A, Z(F_{l+1})\bigr).$$

Hence $l+1 > \mathcal{D}_1(A)+2$ and $\mathcal{D}_1(A,l) \leqslant l+1$.

If $r \geqslant F_l + 1$, then (i) implies the contradiction

$$\mathcal{D}_1(A,l) \leqslant l+1 \leqslant \mathcal{D}_1\big(Z(F_l+1)\big)+1 \leqslant \mathcal{D}_1\big(Z(r)\big)+1 \leqslant \mathcal{D}_1\big(A, Z(F_{l+1})\big).$$

Therefore, $r \leqslant F_l$ which implies $F_{l+1} - r \geqslant F_{l-1}$. Again by (i), we obtain the contradiction

$$\begin{aligned}\mathcal{D}_1(A,l) &\leqslant l+1 \leqslant \mathcal{D}_1\big(Z(F_{l-1}+1)\big)+2 \leqslant \mathcal{D}_1\big(A, Z(F_{l-1})\big)+2 \\ &\leqslant \mathcal{D}_1\big(A, Z(F_{l+1})\big).\end{aligned}$$

This final contradiction completes the proof of (ii).

(iii) This proof is very similar to the proof of (ii) and we just include it for the sake of completeness. For contradiction, we assume that (l, B) is a counterexample of minimum length $1+m$.

As before, this implies that there is some $1 \leqslant r \leqslant F_{l+2} - 1$ such that

$$\mathcal{D}_1\big(Z(F_{l+2}), B\big) = \max\big\{\mathcal{D}_1\big(Z(r)\big)+2, \mathcal{D}_1\big(Z(F_{l+2}-r), B\big)+1\big\}. \tag{8}$$

By (6), we have $\mathcal{D}_1(l, B) \leqslant \max\{l+2, \mathcal{D}_1(B)+1\}$.

If $\mathcal{D}_1(B)+1 \geqslant l+2$, then (8) implies the contradiction

$$\mathcal{D}_1(l,B) \leqslant \mathcal{D}_1(B)+1 \leqslant \mathcal{D}_1\big(Z(F_{l+2}-r), B\big)+1 \leqslant \mathcal{D}_1\big(Z(F_{l+2}), B\big).$$

Hence $l+2 > \mathcal{D}_1(B)+1$ and $\mathcal{D}_1(l,B) \leqslant l+2$.

If $r \geqslant F_l + 1$, then (i) implies the contradiction

$$\mathcal{D}_1(l,B) \leqslant l+2 \leqslant \mathcal{D}_1\big(Z(F_l+1)\big)+2 \leqslant \mathcal{D}_1\big(Z(r)\big)+2 \leqslant \mathcal{D}_1\big(Z(F_{l+2}), B\big).$$

Therefore, $r \leqslant F_l$ which implies $F_{l+2} - r \geqslant F_{l+1}$. Again by part (i), we obtain the contradiction

$$\begin{aligned}\mathcal{D}_1(l,B) &\leqslant l+2 \leqslant \mathcal{D}_1\big(Z(F_{l+1}+1)\big)+1 \\ &\leqslant \mathcal{D}_1\big(Z(F_{l+1}), B\big)+1 \leqslant \mathcal{D}_1\big(Z(F_{l+2}), B\big).\end{aligned}$$

This final contradiction completes the proof of (iii).

(iv) For contradiction, we assume that (A, l, B) is a counterexample of minimum length $n+1+m$.

As before, this implies that there is some $1 \leqslant r \leqslant F_{l+3} - 2$ such that

$$\begin{aligned}&\mathcal{D}_1\big(A, Z(F_{l+3}-1), B\big) \\ &\quad = \max\big\{\mathcal{D}_1\big(A, Z(r)\big)+2, \mathcal{D}_1\big(Z(F_{l+3}-1-r), B\big)+1\big\}.\end{aligned} \tag{9}$$

If $r \geqslant F_{l+1}$, then (6), (9) and (ii) imply the contradiction

$$\begin{aligned}\mathcal{D}_1(A,l,B) &\leqslant \max\big\{\mathcal{D}_1(A,l)+2, \mathcal{D}_1(B)+1\big\} \\ &\leqslant \max\big\{\mathcal{D}_1\big(A, Z(F_{l+1})\big)+2, \mathcal{D}_1(B)+1\big\} \\ &\leqslant \max\big\{\mathcal{D}_1\big(A, Z(r)\big)+2, \mathcal{D}_1\big(Z(F_{l+3}-1-r), B\big)+1\big\} \\ &= \mathcal{D}_1\big(A, Z(F_{l+3}-1), B\big).\end{aligned}$$

Therefore, $r \leqslant F_{l+1} - 1$ which implies that $F_{l+3} - 1 - r \geqslant F_{l+2}$ and (6), (9) and (iii) imply the contradiction

$$\begin{aligned}
\mathcal{D}_1(A, l, B) &\leqslant \max\bigl\{\mathcal{D}_1(A) + 2, \mathcal{D}_1(l, B) + 1\bigr\} \\
&\leqslant \max\bigl\{\mathcal{D}_1(A) + 2, \mathcal{D}_1\bigl(Z(F_{l+2}), B\bigr) + 1\bigr\} \\
&\leqslant \max\bigl\{\mathcal{D}_1\bigl(A, Z(r)\bigr) + 2, \mathcal{D}_1\bigl(Z(F_{l+3} - 1 - r), B\bigr) + 1\bigr\} \\
&= \mathcal{D}_1\bigl(A, Z\bigl(F_{l+3} - 1\bigr), B\bigr).
\end{aligned}$$

This final contradiction completes the proof of (iv). □

Theorem 1. *If* $a_1, a_2, \ldots, a_n \in \mathbb{N}_0$, *then*

$$\begin{aligned}
\mathcal{D}_1(a_1, a_2, \ldots, a_n) &\leqslant \mathcal{D}_1\left(Z\left(\sum_{i=1}^{n}(F_{a_i+3} - 1)\right)\right) \\
&< \log_{\frac{\sqrt{5}+1}{2}}\left(\sum_{i=1}^{n} 2^{a_i}\right) + 2 \approx 1.44 \log_2\left(\sum_{i=1}^{n} 2^{a_i}\right) + 2.
\end{aligned}$$

Proof. The first inequality follows immediately from Lemmas 3 and 4(iv).

By Lemma 4(i), $\mathcal{D}_1(Z(l)) = k$ implies that $l > F_k \geqslant (\frac{\sqrt{5}+1}{2})^{k-2}$ for $k \in \mathbb{N}$ and $l \in \mathbb{N}$. Therefore, $\mathcal{D}_1(Z(l)) < \log_{\frac{\sqrt{5}+1}{2}}(l) + 2$. Since $F_{i+3} - 1 \leqslant 2^i$ for $i \in \mathbb{N}_0$, the remaining inequalities follow. □

Corollary 1. *If* $a_1, b_1, a_2, b_2, \ldots, a_n, b_n \in \mathbb{N}_0$, *then*

$$\begin{aligned}
\mathcal{D}_0(a_1, b_1, a_2, b_2, \ldots, a_n, b_n) &< \log_{\frac{\sqrt{5}+1}{2}}\left(\sum_{i=1}^{n}(2^{a_i} + 2^{b_i})\right) + 3 \\
&\approx 1.44 \log_2\left(\sum_{i=1}^{n}(2^{a_i} + 2^{b_i})\right) + 3.
\end{aligned}$$

Proof. By Lemma 3 and Theorem 1, we obtain

$$\begin{aligned}
&\mathcal{D}_0(a_1, b_1, a_2, b_2, \ldots, a_n, b_n) \\
&\quad = \mathcal{D}_1\bigl(\max\{a_1, b_1\} + 1, \max\{a_2, b_2\} + 1, \ldots, \max\{a_n, b_n\} + 1\bigr) \\
&\quad = \mathcal{D}_1\bigl(\max\{a_1, b_1\}, \max\{a_2, b_2\}, \ldots, \max\{a_n, b_n\}\bigr) + 1 \\
&\quad < \log_{\frac{\sqrt{5}+1}{2}}\left(\sum_{i=1}^{n} 2^{\max\{a_i, b_i\}}\right) + 3 \\
&\quad < \log_{\frac{\sqrt{5}+1}{2}}\left(\sum_{i=1}^{n}(2^{a_i} + 2^{b_i})\right) + 3
\end{aligned}$$

and the proof is complete. □

5. Algorithm for f as in (1)

We now describe the algorithm for functions f as in (1).

Algorithm 2.
Input: A function f with inputs $x_1, x_2, \ldots, x_n$ as in (1) specified by gates $g_1, g_2, \ldots, g_{n-1} \in \Omega$ and an arrival time $t(x_i)$ for x_i for $1 \leqslant i \leqslant n$.
Output: A circuit C_f for f over Ω.

Step 1 Set $t_1 \leftarrow t(x_1)$ and $s_1 \leftarrow 0$.
For $1 \leqslant i \leqslant n-1$ set $t_{i+1} \leftarrow t(x_{i+1})$ and $s_{i+1} \leftarrow 0$, if $g_i = \vee$.
For $1 \leqslant i \leqslant n-1$ set $t_{i+1} \leftarrow 0$ and $s_{i+1} \leftarrow t(x_{i+1})$, if $g_i = \wedge$.

Step 2 Use Algorithm 1 to construct the circuit $C_{0,f_0}(t_1, s_1, t_2, s_2, \ldots, t_n, s_n)$ on the inputs x_1', x_1'', x_2', x_2'', $\ldots$, x_n', x_n'' with arrival times t_i for x_i' and s_i for x_i'' for $1 \leqslant i \leqslant n$.

Step 3 Set $x_1' \leftarrow x_1$ and $x_1'' \leftarrow 1$.
For $1 \leqslant i \leqslant n-1$ set $x_{i+1}' \leftarrow x_{i+1}$ and $x_{i+1}'' \leftarrow 1$, if $g_i = \vee$.
For $1 \leqslant i \leqslant n-1$ set $x_{i+1}' \leftarrow 0$ and $x_{i+1}'' \leftarrow x_{i+1}$, if $g_i = \wedge$.

Step 4 The circuit C_f arises from the circuit constructed so far by eliminating all constant inputs using the relations $x \vee 0 = x \wedge 1 = x$, $x \vee 1 = 1$ and $x \wedge 0 = 0$.

Lemma 5. *Algorithm 2 works correctly and can be implemented to run in cubic time.*

Proof. Using the identities $x \vee y = (x \vee y) \wedge 1$ and $x \wedge y = (x \vee 0) \wedge y$, it is straightforward to check that C_f computes f (cf. Fig. 5). Hence Algorithm 2 works correctly. Its time complexity follows from the time complexity of Algorithm 1 and the fact that considering each of the less than $8n-3$ $\vee$- or $\wedge$-gates of $C_{0,f_0}(t_1, s_1, t_2, s_2, \ldots, t_n, s_n)$ once in non-increasing distance from the output gate, step 4 can be done in linear time. $\square$

Theorem 2.

(i) *If C_{0,f_0} denotes the circuit generated by Algorithm 1 for f_0 as in (3) given arrival times for the inputs, then* $\mathrm{delay}(C_{0,f_0}) \leqslant 1.44\,\mathrm{delay}(f_0) + 3$.

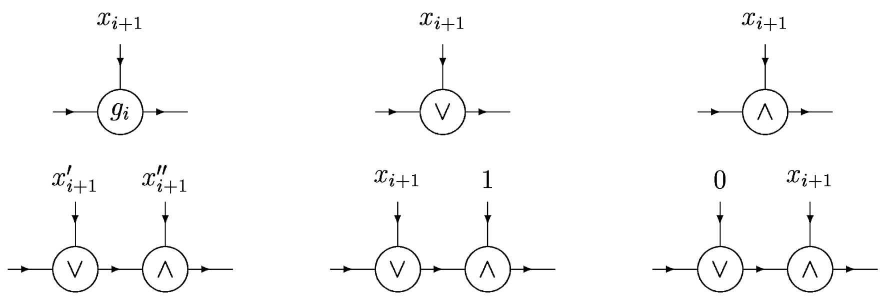

Fig. 5.

(ii) *If C_f denotes the circuit generated by Algorithm 2 for f as in (1) given arrival times for the inputs, then* $\text{delay}(C_f) \leqslant 1.44\,\text{delay}(f) + 4.44$.

Proof. (i) This follows immediately from Lemma 1 and Corollary 1.

(ii) Using the same notation as above, we have

$$\sum_{i=1}^{n}(2^{t_i} + 2^{s_i}) \leqslant 2\sum_{i=1}^{n} 2^{t(x_i)}.$$

By Lemma 1 and Corollary 1, we obtain

$$\begin{aligned}
\text{delay}(C_f) &\leqslant \text{delay}\big(C_{0,f_0}(t_1, s_1, t_2, s_2, \ldots, t_n, s_n)\big) \\
&\leqslant 1.44\log_2\left(\sum_{i=1}^{n}(2^{t_i} + 2^{s_i})\right) + 3 \\
&\leqslant 1.44\log_2\left(2\sum_{i=1}^{n} 2^{t(x_i)}\right) + 3 \\
&\leqslant 1.44\log_2\left(\sum_{i=1}^{n} 2^{t(x_i)}\right) + 4.44 \\
&\leqslant 1.44\,\text{delay}(f) + 4.44
\end{aligned}$$

and the proof is complete. □

6. Conclusion

We have described a simple cubic-time algorithm for the construction of circuits for functions as in (1) whose delay is at most 1.44 times the lower bound plus some small constant. Our algorithm is essentially the first mathematically justified method that allows for the redesign of the logic on longer critical paths at late stages of the VLSI design process.

As we mentioned, the functions as in (3) are closely related to addition. As a consequence, we can construct circuits over the basis $\{\vee, \wedge, \neg\}$ for the addition of two binary n-digit numbers whose delay is at most 1.44 times the optimal delay plus some small constant. Unfortunately, the number of gates of these circuits is quadratic in n. In [8] we describe circuits for the same task whose delay is essentially at most twice the lower bound and whose size is $\mathrm{O}(n\log(\log(n)))$.

In view of the practical motivation explained in the first section, it is obvious that many technical details not contained in the mathematical abstraction can actually be incorporated in the algorithm. This motivation is also the reason for controlling the number of gates and the maximum fan-out.

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